SYNOPSYS®

DATASHEET

Static Verification CoStart: RTL Signoff

VELOCITY

Accelerate RTL signoff with Synopsys tool and methodology experts

Overview

With the increasing SoC design complexity for mobile, artificial intelligence and advanced applications, there is an exponential increase in the number of clocks and resets in a design. Increased interdependence among clock domains, reset domains, and power domains has led to multifold increase in design verification complexity. This has necessitated targeted verification to address the interaction of clock, resets, and power domains.

This increase in SoC complexity demands correct by construction RTL, Synopsys Design Constraints (SDC) with clock domain crossings (CDC), and reset domain crossings (RDC) verified early in the RTL development phase.

Synopsys VC SpyGlass™ platform enables designers to analyze RTL designs early in the design flow, with minimal setup effort and without the need for testbench or stimulus. This allows bugs to be found and fixed early, reducing overall cost, time, and effort by eliminating respins.

Today, leading SoC design teams use RTL Linting, SDC, CDC or RDC checks in their verification flows. While many users are well-versed in these methodologies, others are still ramping up, which is impacting their project schedules and potentially leaving bugs undetected.

Static Verification CoStart for Best-in-Class RTL Signoff

Verification CoStart enables SoC design teams to accelerate adoption of static verification technologies and increase productivity in their verification environments.

Verification CoStart for RTL Signoff is a 10-day service where Synopsys engages with the customers to accelerate their knowledge of Lint, CDC, and RDC techniques leveraging the Synopsys VC SpyGlass platform. Synopsys consultants will assist the customer's design team in setting up the RTL static signoff methodology and help in faster verification closure.

Synopsys' expert consultants will help set up the methodology and flow on a few design blocks to ensure that design and verification engineers can leverage the tools in production early. To complete the services engagement, Synopsys will provide hands-on training on how-to run the tool, debug, and interpret results for up to five engineers.

Verification CoStart RTL Signoff Services

As part of the engagement, Synopsys experts will work closely with customer's engineers to enable the following:

- Overview of Lint, CDC, and RDC verification with clean design constraints
- Design bring-up for running VC SpyGlass
- VC SpyGlass Lint Methodology
  - Execute Synopsys GuideWare™ Lint methodology on design and Lint cleanup review
  - Running Functional Lint analysis for noise reduction
- VC SpyGlass CDC Methodology
  - Defining design constraints for CDC verification
  - Executing CDC setup checking
  - Review unsynchronized and synchronized crossings
  - Achieving glitch and convergence analysis
  - Debugging in Verdi® coupled with how-to fix CDC problems
  - Running hierarchical Signoff Abstract Model (SAM) flow
  - Using machine learning based root cause analysis (ML-RCA) feature
- VC SpyGlass RDC Methodology
  - Defining setup methodology (skip reset, others)
  - Constraining design for RDC checking
  - RDC setup checking
  - Reviewing unsynchronized and synchronized crossings
  - Debugging in Verdi debug and how-to fix RDC problems
  - Using hierarchical Signoff Abstract Model (SAM) methodology

Assumptions and Dependencies

- Customer's design engineers will be available for consultation with Synopsys consultants
- Synopsys will have access to customer's design environment either directly or through a customer's engineer
- Customer has identified the engineers who will go through the hands-on training program

For more information about Synopsys products, support services or training, visit us on the web at www.synopsys.com, contact your local sales representative or call 650.584.5000

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