SLM Signal Integrity Monitor

Measure Signal Quality of Silicon Interconnects

Highlights

- Die-to-die interface signal margin measurement from rising/falling edge to clock transition
- Supports SDR and DDR interfaces
- Primarily targeted for UCIe and HBM PHYs
- Low overhead for data processing
- EDA integration for automated insertion and connection
- Capture state of silicon precisely at any stage of its lifecycle
- Available as hard IP integrated with PHY or soft IP with flexibility to customize

Use Cases

- Die-to-die interface monitoring
- 1D eye diagram creation
- Monitor, Test and Repair (MTR) of UCIe PHY in-test or in-field

Overview

Synopsys SLM Signal Integrity Monitor (SIM) IP enables signal quality measurement for die-to-die interfaces. It can be implemented in silicon with minimal area overhead. It enables accurate measurement of silicon interconnects with real-time reporting for analytics. With the use of Monitor, Test and Repair (MTR), this real-time reporting enables structural lane monitoring, aging related degradation, and optional repair of failing lanes to maintain high-speed performance throughout the silicon lifecycle.

The SIM unit (SIMU) has a capture mode for reporting the positive and negative margin of signal edge relative to clock edge. It can support SDR and DDR formats with a clock forwarding scheme. Typically, one SIMU is connected at the end of each lane and all the SIMU's form a chain connecting to the SIM controller (SIMC). The SIMC provides control /status and test access via 1500/1687.

Information collected from the SIM can be used to construct a 1D eye diagram and based on that, the PHY's test and repair scheme can be implemented. SLM SIM IP supports SDR and DDR interfaces with UCIe, with HBM interfaces being primary applications. Signal integrity monitor units (SIMU) combined with a signal integrity monitor controller (SIMC) form a complete solution for a multi-die package. Scan chain, IEEE 1500/1687 is available via SIMC. SLM SIM IP is available as a hard macro integrated with UCIe, HBM PHYs from Synopsys or as configurable soft IP.

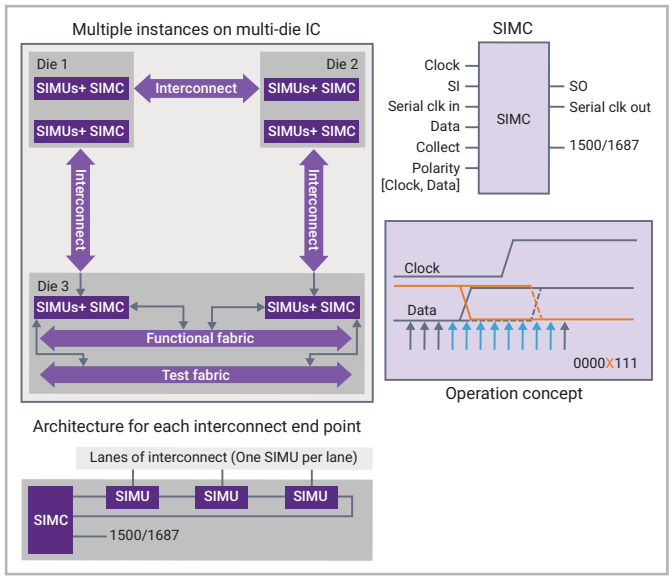

Figure 1: Synopsys SLM Signal Integrity Monitor (SIM) IP

SLM Structural Monitors

Structural monitors are key to the success of Synopsys' Silicon Lifecycle Management solution. These monitors are embedded in the silicon and report out the health of critical functions of the chip. Data from structural monitors can be collected at any stage of the silicon lifecycle and analyzed to gather insights. Based on these insights, actions can be taken to improve performance or mitigate an operational issue. Memory, CPU workload, interface, clock, delay, etc. are some critical functions on an SoC worth monitoring. Synopsys' structural monitors are enabled with EDA and software automation for ease of use.

Key Features

- SIMU + SIMC based complete solution for multi-die packages
- Distributed architecture with low overhead
- Available as hard IP integrated with PHY or soft IP with flexibility to customize
- Capture state of silicon at any stage of its lifecycle

Key Benefits

- Health check of die-to-die interfaces within 3DIC
- Interface signal timing margin measurement
- Monitor, Test and Repair (MTR) of PHY in-test or in-field
- Optimize silicon performance for safety critical applications

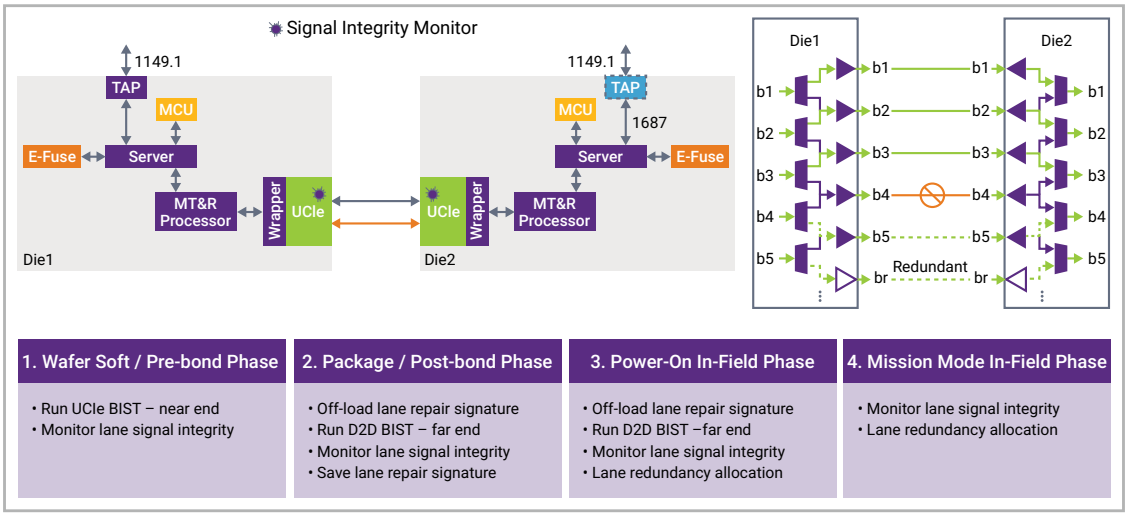

Figure 2: Complete solution in SHS environment for UCIe Interface Monitor, Test and Repair

About Synopsys IP

Synopsys is a leading provider of high-quality, silicon-proven semiconductor IP solutions for SoC designs. The broad Synopsys IP portfolio includes logic libraries, embedded memories, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate IP integration, software development, and silicon bring-up, Synopsys' IP Accelerated initiative provides architecture design expertise, pre-verified and customizable IP subsystems, hardening, and signal/power integrity analysis. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market.

For more information on Synopsys IP, visit synopsys.com/ip.