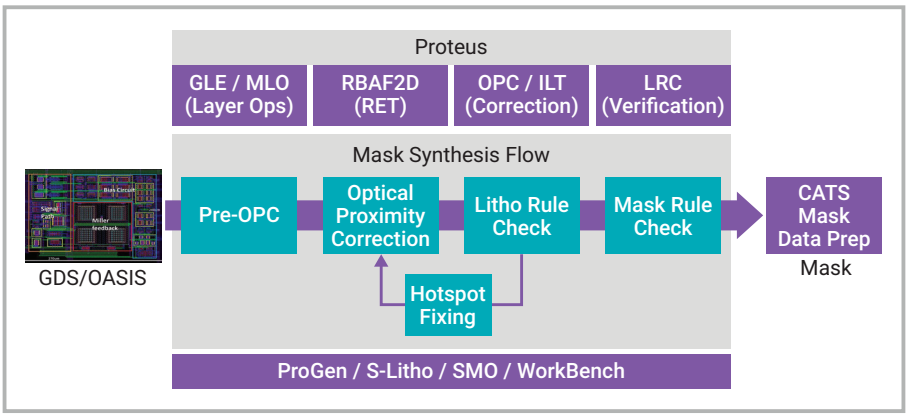
SYNOPSYS®

DATASHEET

Proteus

Full-Chip Mask Synthesis

Proteus provides a complete suite of leading-edge lithography solutions for mask synthesis to model the manufacturing process, perform lithography process optimization, provide full-chip correction of proximity effects, and detect design locations that are sensitive to process variability (hotspots). For development and production use models, Proteus and S-Litho, our rigorous physics-based lithography simulator, have been tightly integrated to provide the industry's highest level of accuracy and predictability to deliver faster time-to-market results. Synopsys' Mask Synthesis tools have been industry tested for over two decades and are the tool of choice for leading-edge IDM's and foundries.



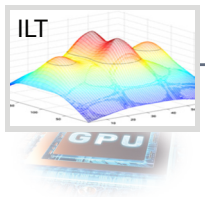
Benefits

- Complete solutions for both development and manufacturing
- Captures largest lithography entitlement with industry's most widely production deployed ILT solution
- Fast turnaround time with AI driven solutions utilizing the latest CPU/GPU/Cloud hardware
- Superior hierarchy compression for most efficient use of compute resources
- Highly predictive 3D resist and mask models
- Industry's only mask synthesis tool set with integrated support for rigorous physics-based models through S-Litho
- Core technology uniquely connects manufacturing information to design, manufacturing and yield analytics
- Full support for all lithography processes including the latest immersion and high NA EUV processes

Applications

Proteus Optical Proximity Correction (OPC) provides the fast and accurate model-based optical proximity correction with flexible support for Manhattan and the latest curvilinear flows. OPC utilizes discrete evaluation sites in the space domain to correct the polygon edges for the fastest correction times. The curvilinear correction capabilities handle more challenging dense designs with less restriction from mask rule constraints for better correction convergence, larger process windows, and improved wafer quality.

Proteus Inverse Lithography Technology (ILT) is the industry's first and most widely production deployed inverse lithography solution, providing the largest process windows, higher yield, and faster time to market while delaying the need for costly new hardware and multipatterning technologies. ILT provides the most advanced correction capabilities to address the most difficult proximity errors. Utilizing a field-based solver to concurrently optimize the main feature correction and assist feature placement, ILT natively supports the latest curvilinear flows. Capturing the largest process entitlement, it delivers the highest level of wafer quality with full MRC compliance for the latest advanced EUV layers while also supporting Manhattan flows for less critical layers. The flexible cost functions support a wide range of optimization capabilities from process window, litho/mask co-optimizations, automated pitch relaxation on routing layers and localized hotspot fixing with blending into existing OPC.



	Feature	Application
PW ILT	Process Window Optimization • AF and main co-optimization • Maximizes common process window	• Memory cell/core, hotspot fixing for logic & memory periphery, and full chip
TOP-ILT	Target Optimization • Mask and target co-optimization • Improves image contrast	• Localized hotspot fixing and full chip
Rig. ILT	Rigorous Correction • Resist 3D aware correction • Reduces resist top-loss	• Memory cell and hotspot fixing with S-Litho (rigorous simulations)
Curve ILT	Curve Correction • Curve design & mask support • Better process correction, CD uniformity, and process window	• Memory cell/core, display pixel region, hotspot fixing, and full chip
ML ILT	Machine Learning Correction • AI Assisted Correction • Faster processing times	• Memory cell, logic, and full chip

Proteus Global Layer Enhancer (GLE) provides a comprehensive set of full field global layer operations for pre-OPC data prep, including primitive polygon manipulation, and table-driven biasing/rule-based OPC with efficient hierarchy management for fastest handoff to downstream Proteus applications. GLE supports fast consistent correction flows and quick resolution of yield-killing design sensitivities with a comprehensive pattern matching engine.

Proteus Rule-Based Assist Feature 2D (RBAF2D) provides geometric table-driven placement of sub-resolution assist features to address the print bias between isolated and dense features and enable a larger common depth of focus. Proteus RBAF2D provides assist feature coverage for 1D and 2D regions. Included is a model assisted rule table (MART) utility that utilizes Proteus' industry leading ILT solution to establish optimal rules for faster AF rule creation.

Proteus Lithography Rule Check (LRC) provides post OPC verification tools for full chip mask validation with industry-leading accuracy. Proteus LRC delivers fast comprehensive hotspot, two-layer spacing and overlay, stitching, process variability, EPE, and CD control checking capabilities through the process window to quickly identify hotspots to support more robust design practices and hotspot resolution prior to committing a design to mask manufacture.

Proteus Source Mask Optimization (SMO) identifies the optimal illumination source shape for any set of critical patterns or cells, while simultaneously tuning the mask for best lithographic performance. The cost function can be flexibly defined by the user and quality assessments made with LRC functionality using gauge- or field-based assessment. For the mask treatment, production proven ILT recipes are deployed, which ensures a smooth transfer of the SMO specific mask solution to full chip mask synthesis applications.

Proteus WorkBench (PWB) is Synopsys' powerful cockpit tool for development and optimization of Proteus-based mask synthesis solutions. It is based on an effective hierarchical GDSII/OASIS layout visualization engine, providing a comprehensive environment for lithography simulation, compact model building, full-chip optical proximity correction (OPC) recipe tuning, layout verification, and mask synthesis flow development. PWB also supports the development and assessment of resolution enhancement techniques (RETs), resulting in a fast turnaround time for setting up production-ready mask synthesis flows.

Proteus ProGen models are empirical compact models reflecting the performance of a lithography process. Model parameters are determined by fitting experimental data. The Proteus Modeling Platform (PMP) provides a single environment for calibrating those parameters with a high degree of automation and tuning them for optimum performance in downstream applications.

Sentaurus™ Lithography (S-Litho) represents the industry standard in lithography simulation for semiconductor process development and optimization in advanced memory and logic applications. It covers a wide range of patterning techniques, from proximity printing to high NA EUV lithography. Using physics-based models, S-Litho predicts the outcome of a lithographic process, such as the 3D resist profile or a process window. Interfacing S-Litho with TCAD tools such as Sentaurus Topography enables seamless modeling of complex integration techniques such as double-patterning. The link between S Litho and Proteus™ tools accelerates the development of optical proximity correction (OPC) solutions and supports the verification flow through automated hotspot analysis, significantly reducing cycle time.

For more information please contact your local sales representative or email us at manufacturing@synopsys.com.

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