SYNOPSYS®
Silicon to Software™

Proteus LRC

Full-Chip Verification Through Process Window

Overview

Proteus LRC (lithography rule check) is Synopsys' post-optical proximity correction (OPC) verification tool enabling fast and accurate hotspot detection across the process window for full-chip mask validation within the highly-scalable Proteus Pipeline Technology. Problem areas are quickly identified, enabling more robust design and OPC practices early in the development cycle while reducing the risk of device failure later during the production flow. Improve time to market for new technologies and increase yield for existing flows with Proteus LRC.

As lithography processes approach the resolution limits of existing toolsets, devices become more susceptible to failure due to increased variation through the process window and tighter tolerances associated with smaller design nodes. Proteus LRC provides fast comprehensive hotspot, two layer spacing and overlay, EPE, and CD control checking capabilities through the process window. Rigorous checking and analysis capabilities available within Proteus LRC enable identification of potential sources of yield loss before committing designs to manufacture, saving time and costly mask re-spins.

Proteus LRC delivers industry leading accuracy with process window-aware error detection and production-proven models for a reliable and comprehensive process verification solution. A fully customizable interface provides unparalleled flexibility, allowing users to incorporate their own algorithms without having to compromise their IP. The application is fully integrated into the Proteus Pipeline Technology and runs on standard x86 core processors for the best cost of ownership, while the advanced error analysis capabilities provide tools for the most efficient review and disposition of results.
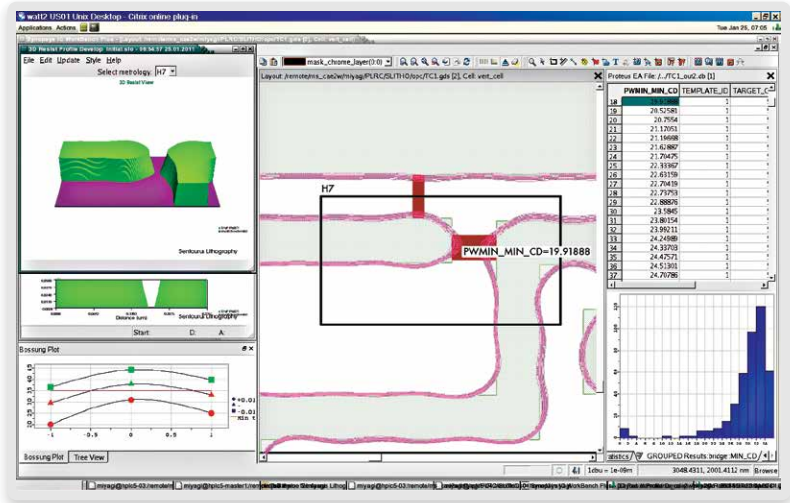

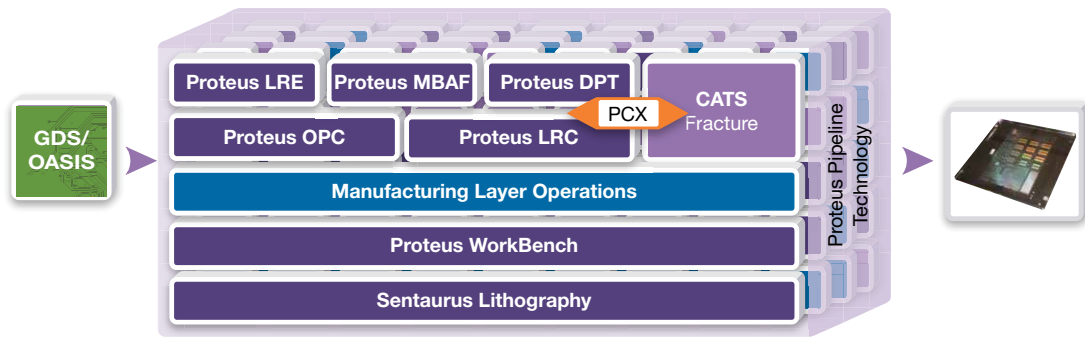**Figure 1. Proteus Error Analysis Module in IC WorkBench**

Figure 2. Proteus Pipeline Technology

Industry Leading Accuracy

The same production-proven models used by Proteus OPC are used by Proteus LRC. These models use advanced resist profile modeling techniques, providing the best foundation for highly accurate and predictable models through the process window. This has resulted in superior model stability, providing industry-leading accuracy even when results extend outside the range of the model calibration data. When additional insight into the resist profiles and topography affects are required, embedded Sentaurus Lithography technology provides access to rigorous first-principle models for those critical locations in a design.

Process Window-Aware Error Detection With Unparalleled Flexibility

Proteus LRC provides full-chip coverage with advanced field-based models.

▸ All checks employ process window-aware algorithms for optimal performance and consolidated data analysis by identifying the worst error across the process window for any location in a design

▸ DPT-specific check functions are optimized for the unique process errors encountered in a multi-mask lithography process, thereby providing robust checking, easy implementation, and consolidated results viewing

▸ Embedded Sentaurus Lithography technology provides easy access to resist profiles and topography effects through rigorous first principle models

▸ Standardized platform between OPC and Proteus LRC provides a consistent syntax for easy transitioning between tools

▸ Fully programmable interface maintains Synopsys' renowned level of flexibility, allowing the end user to incorporate their own check functions and algorithms to protect user's valuable IP

▸ Advanced full chip 3D hotspot detection with rigorous S-Litho and compact ProGen resist 3D models

Advanced Error Analysis

As shown in Figure 1, the Proteus Error Analysis Module within Synopsys' Proteus WorkBench provides an intuitive and feature-rich GUI environment for driving to error locations, reviewing histograms, statistical summaries, Bossung plots, and 3D resist profile and topography analysis. An industry-standard database format is employed for efficient and full flexibility in viewing, querying and summarizing results for custom applications

▸ Errors are grouped across the process window and based on context for more compact/efficient error reviewing

▸ Full-chip statistical analysis of all parameters checked

▸ Data handoff to wafer and mask inspection tools

Best Cost of Ownership

As displayed in Figure 2, Proteus LRC runs on the Proteus Pipeline Technology for superior performance and scalability on standard hardware, providing fast turn-around-time with low cost of ownership. The entire mask synthesis flow is executed with a single job deck providing concurrent processing of all stages in the flow for the most efficient CPU utilization.

For more information about Synopsys products, support services or training, visit us on the web at: www.synopsys.com, contact your local sales representative or call 650.584.5000.